

Applicant(s): Soo-geun Lee, *et al.*
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forming a first interlayer insulating layer on the first etching stopper;
forming a second interlayer insulating layer over the first etching stopper;
etching the second interlayer insulating layer and the first interlayer insulating layer sequentially using the first etching stopper as an etching stopping point to form a via hole aligned with the lower conductive layer;

forming a protective layer to protect a portion of the first etching stopper exposed at the bottom of the via hole, the protective layer filling the via hole and extending across the via hole;

removing the protective layer;

removing the portion of the first etching stopper positioned at the bottom of the via hole; and

forming an upper conductive layer that fills the via hole and the trench and is electrically connected to the lower conductive layer.

6. (Amended) The method of claim 19, wherein the second etching stopper is formed of at least one of silicon nitride and silicon carbide.

Please add the following new claims.

19. (New) The method of claim 1, further comprising forming a second etching stopper on the first interlayer insulating layer.

20. (New) The method of claim 19, wherein the etching step further comprises etching the second etching stopper with the second interlayer insulating layer and the first interlayer insulating layer using the first etching stopper as an etching stopping point to form the via hole aligned with the lower conductive layer.

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21. (New) The method of claim 19, further comprising etching a portion of the second interlayer insulating layer adjacent to the via hole using the second etching stopper as an etching stopping point to form a trench connected to the via hole.